

# Speed improvements in power supply test

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**Technology advances in power supply test equipment hardware and software offer manufacturers the possibility to make significant improvements in test speed accuracy.**

This article examines the issues, which affect throughput in PSU (power supply unit) test, with special reference to a new test concept developed by Intepro. It offers examples of some leading power supply manufacturers in Asia and Europe who have achieved significant increases in test speed using Intepro's new Intepro 9000 advanced test system.

## Handling

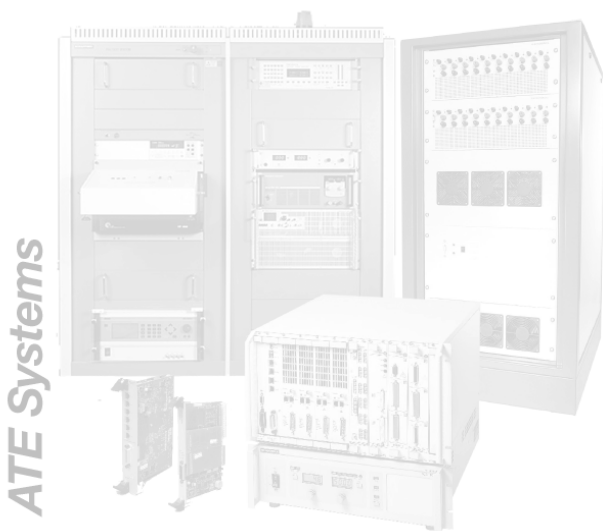
As technology advances and test times are reduced, the time required for handling and loading boards is becoming critical to throughput in some test installations. Leading manufacturers are increasingly considering the use of automated handling systems, electronic bar-code readers and multi-well fixtures in the test area, in the drive to maximise throughput.

## Test methodology

Intepro's research has identified two factors key to the minimising of test times. One is the duplication of measurements in the test programme. The other is power supply settling times.

## Eliminating measurement duplication

Traditionally, ATE software allowed the user to set-up a sequence of tests, which were saved into a test programme. When the programme was executed, the software implemented each test in turn by allowing the unit to settle to the appropriate state, taking the required measurements, and logging the results.



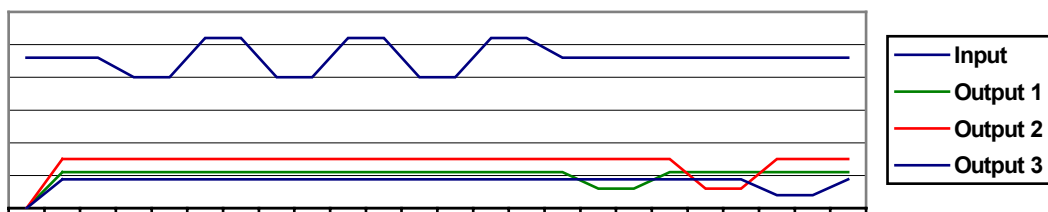
**Figure 1: Typical Test Program**

Test Name	UUT State			
	Input V	Output 1	Output 2	Output 3
Ramp Up	Set Input V			
Setup test Conditions		Set Load	Set Load	Set Load
Input Current	Read I			
Output Voltage 1		Read V		
Output Voltage 2			Read V	
Output Voltage 3				Read V
Efficiency	Read I & V	Read I & V	Read I & V	Read I & V
Line Regulation OP 1	Set Line Low	Read V		
	Set Line High	Read V		
Line Regulation OP 2	Set Line Low		Read V	
	Set Line High		Read V	
Line Regulation OP 3	Set Line Low			Read V
	Set Line High			Read V
Load Regulation OP 1		Set Load	Set Load	Set Load
		Read V		
Load Regulation OP 2		Set Load	Set Load	Set Load
			Read V	
Load Regulation OP 3		Set Load	Set Load	Set Load

Figure 1 shows a typical test programme for a three-output AC/DC converter, including input current, voltage, efficiency, line regulation and load regulation tests. It shows clearly the duplication of measurements typical of traditional test programming. For example, the efficiency test repeats measurements already made for the output voltage and input current tests.

Figure 2 shows the changes in state of the power supply unit during the test. Every time the state is changed, the test programme has to wait for the unit to settle before measurements can be taken.

**Figure 2 UUT State Changes**



Intepro's new test concept eliminates this duplication of measurement using a series of 'acquire' tests to measure and store all the values required for the test programme. Each measurement is performed only once, and the power supply unit passes through each state change only once. The measured values are then made available to a series of evaluation tests which calculate the required results such as output voltage, load regulation, line regulation, efficiency and so on.

As an example of the test time savings achievable with this approach, consider a line regulation test on a DC-DC converter power supply with multiple outputs:

- Line regulation =  $\text{abs}(V_o - V_1) \times 1000$

Where:

$V_o$  = output voltage at maximum input voltage

$V_1$  = output voltage at minimum input voltage

Under the traditional approach, each set of measurements would have to be made for each output, at *line-high* (maximum input voltage) and *line-low* (minimum input voltage) settings.

- Test time = (source settling time + PSU settling time + measurement time) x 2 x no outputs

Using the new concept, the low line level is set and the output voltages are measured, then the high line level is set and the outputs are measured again.

- Test time = (source settling time + PSU settling time) x 2 + (measurement time x 2 x no outputs)

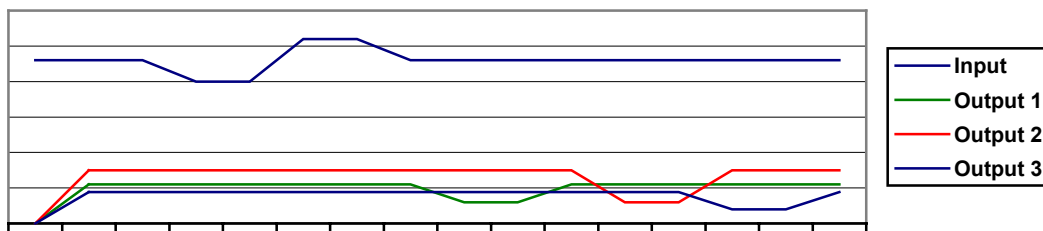
If the source settling time is 20ms, PSU settling time is 25ms and measurement time is 20ms (for example), then for a five output power supply, the time to carry out the line regulation is reduced from 650ms to 290ms by using this method. This is a test time saving of more than 40%.

Note: Further test time savings can be made by using the method described above to measure the maximum and minimum input voltages and store the results in memory for reference by other tests in the programme.

### Minimising PSU settling times

As demonstrated above, eliminating duplication of measurement means that duplication of the associated settling times is also eliminated. Figure 3 shows the changes in state of the power supply unit during the test using the new concept. This alone has a significant impact on the total test time, but it can be further improved by reducing to a minimum the amount of time allowed by the programme for settling of the PSU.

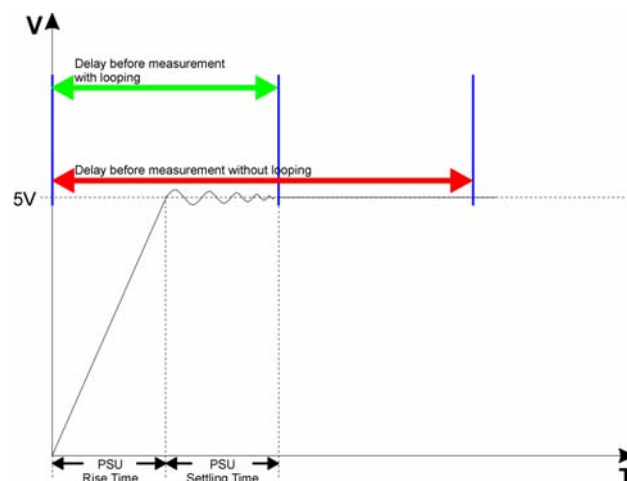
Figure 3 UUT State Changes



Traditionally, ATE test software allowed a predefined, fixed amount of time for the PSU to settle following a state change, before making a measurement. The settling times allowed were based on experience and gave a sensible margin. No measurement was made until after the allotted time. Neither was the settling time allowed related to measurement resolution.

Intepro's new test concept reduces the time allowed for settling to its absolute limit for each individual measurement. A programming loop is used to constantly verify the actual state of the power supply.

Figure 4: Fixed delay before measurement vs. looping technique



As soon as the unit is sufficiently settled to allow the measurement to be made with statistical certainty, according to the resolution as defined by the programme (see **Measurement speed** below), the measurement is implemented. This not only reduces the time allowed in the test for settling, but also improves the accuracy and reliability of the test results.

Figure 4 represents the settling process for a typical DC-DC converter. Conventional ATE methods require an arbitrary fixed time delay before a measurement is taken. By implementing a loop technique to verify the UUT status, the delay can be reduced to an absolute minimum. By reducing the time allowed for settling in this way, significant savings on overall test times can be made.

## **Program development**

In a discussion like this, it is worth remembering that a major factor governing test times in any test environment is the quality of the test programme as developed by the engineer. The ATE software can only make tools available. In practice the skill and expertise of the test engineer to interpret the test specification is paramount.

Time spent generating the programme must be weighed against test time, in the light of production volumes and available resources. For example, test times may be reduced by making sure the test programme requires no operator decisions. Decisions take time, and carry a risk of error. Extra programming time spent creating a series of simple, clear instruction screens can save significant amounts of test time in the long run. These could include a virtual *start* button to invoke the next test programme, for example, or a built-in bar code reader for automatic identification of serial numbers.

## **Measurement speed**

### ***Resolution***

ATE software which gives the test engineer / programmer full control of measurement resolution of the hardware allows further reduction of test times.

There are significant speed advantages to be gained in selecting the most appropriate measurement resolution, according to the test specification. The lower the resolution required, the faster the DVM measurement is made. For example, if tolerances on auxiliary outputs are wider than those on the main output, then a lower resolution may be acceptable for auxiliary measurements. The test time savings to be made may be considerable. Test time for a two-output DC-DC converter from one of Intepro's customers was reduced by 119ms, by optimisation of measurement times alone. This result was typical of those looked at in research.

### ***Scanning***

A single, multi-measurement module helps to increase test speed by eliminating the time required to scan between separate measurement instruments. Where a single module performs four functions - ripple & noise, voltage, resistance and interval timing measurements, for example - signal conditioning and switching time is reduced by 75%.

### ***Parallel measurement***

There is some confusion amongst manufactures of test equipment, and their customers, about the term *parallel measurement* in this context. It is clear that the ability of the ATE to take more than one measurement at a time will improve test speed. However, the term is frequently used to cover a variety of concepts, some of which have more impact on overall test times than others.

The only measurements that can be performed truly 'in parallel' on a single output are ripple & noise and DC output voltage, as these are the only two which require a similar PSU state. Since these are the most time consuming of all PSU measurement operations - requiring averaging of repeated measurements - the potential test time savings are worth considering.

This type of parallel measurement requires a dual-processor measurement module, capable of activating both the ripple and voltage circuits at once. The measurements are made at the same time, and the signals processed simultaneously. Of course, assuming there is only one communications bus from hardware to software, then the measured values are actually delivered to the test program sequentially, but this time difference is not significant.

Likewise, a system which has more than one measurement module may be used to make 'parallel' measurements on more than one output at once, with results delivered sequentially to the PC. This is faster than making the measurements one by one because there are no scanning or other ranging overheads.

In some cases, the term parallel measurement is used to describe the ability to record multiple events, in order to examine one waveform relative to another. For example, a test specification may define a tolerance between the turn-on time for two outputs. If the ATE has two timing circuits, then the two turn-on times can be measured at the same time. If it does not, then the PSU will have to be powered and allowed to settle twice, in order that the two times can be measured.

## Data acquisition

The test procedure is not complete until the results data is logged in a useful format, normally on a central server for direct access by management. It is not uncommon for this logging process to take significantly longer than changeover handling time, so that the operator is delayed momentarily from starting the next test programme run. Over the course of a shift in a high volume test area, the total delay can be significant.

The use of multi-thread processing techniques, to store test results locally for background spooling to a central data manager only when the system is idle, can save as much as 10% of overall test time.

## Examples

In development of its new test concept, Intepro's R&D team has worked closely with power supply manufacturers around the world. The following examples demonstrate the significant time savings that can be made.

- Test times were cut by more than 50% for a US manufacturer of a four-output Japanese-designed telecom power supply. The modular plug-in PSU for network switching systems is manufactured in large volumes, and the test savings represents a significant increase in productivity for the manufacturer.
- Test time for a single output DC-DC converter for a military application were reduced from 12 seconds per unit to just two seconds, using Intepro 9000.
- Test times for a five-output telecom power supply made by an Asian manufacturer were five minutes per unit using a conventional test system. Intepro trials indicate this test time could be cut to just 90 seconds using Intepro 9000.

**Ends**



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